Rev. 1.1, June. 2016

MZVLW128HEGR-00000/07
MZVLW256HEHP-00000/07
MZVLW512HMJP-00000/07
MZVLW1T0HMLH-00000/07

M.2 NVMe PCIe SSD specification

(PM961)

datasheet

SAMSUNG

Revision History

Revision No.	History	Draft Date	Remark	Edited by
1.0	1. Initial issue	May. 23, 2016	Final	Brian Chae
1.1	1. Table 118 changed. 2. 128/256GB performance added.	June. 1, 2016	Final	Brian Chae

PM961 Series

PART NUMBER	MZVLW128HEGR-00000/07	MZVLW256HEHP-00000/07	MZVLW512HMJP-00000/07	MZVLW1T0HMLH-00000/07
Capacity[1]	128GB	256GB	512GB	1TB
LBA[2]	250,069,680	500,118,192	1,000,215,216	2,000,409,264

FEATURES

- PCIe Gen3 8Gb/s Interface, up to 4 Lanes
- Compliant with PCI Express Base Specification Rev. 3.0
- Compliant with PCI Express CEM Specification Rev. 3.0
- Compliant with NVMe Express specification Rev. 1.2 (Partial)
- Power Saving Modes:
  - Supporting APST
  - Supporting L1.2 Mode
- Support Admin & NVM Command Set
- RoHS Compliant
- (-00007 only) TCG Opal (v2.0) Compliant

Environmental Specifications

Temperature	
Operating[4]	0°C to 70°C
Non-operating	-40°C to 85°C
Humidity (non-condensing)	
Non-operating	5 ~ 95%
Linear Shock (0.5ms duration with 1/2 sine wave)	
Non-operating	1,500 Gpeak
Vibration	
Non-operating (10 ~ 2,000 Hz, Sinusoidal)	20 Gpeak

Drive Configuration

Capacity	128/256/512GB/1TB
From Factor	M.2
Interface	PCI Express Gen3 x4
Bytes per Sector	512byte

Performance Specifications [3]

Data Transfer Rate (128KB)	
Sequential Read	(1TB) Up to 3000 MB/s
	(128/256/512GB) Up to 2800 MB/s
Sequential Write	(1TB) Up to 1700 MB/s
	(512GB) Up to 1600 MB/s
	(256GB) Up to 1100 MB/s
	(128GB) Up to 600MB/s
Data I/O Speed (4KB)	
Random Read	(1TB) Up to 360K IOPS
	(512GB) Up to 260K IOPS
	(256GB) Up to 250K IOPS
	(128GB) Up to 140K IOPS
Random Write	(1TB) Up to 330K IOPS
	(512GB) Up to 260K IOPS
	(256GB) Up to 180K IOPS
	(128GB) Up to 40K IOPS

Reliability Specifications

UBER	< 1 sector per 10^{15} bits read
MTBF	1.5 Million Hours

POWER REQUIREMENTS

Supply Voltage / Tolerance	+3.3V ± 5%
Voltage Ripple/Noise (max.)	100mV p-p
Active[5] (Typ, RMS)	
- Read	6.1W
- Write	5.1W
Idle[6] (Typ.)	450mW
L1.2[7] (Typ)	5mW

PHYSICAL DIMENSION

Width	22.00 ± 0.15 mm
Length	80.00 ± 0.15 mm
Height	
(Single Side)	Max. 2.38 mm
Weight	Up to 8 g

Specifications are subject to change without notice.

1) 1MB = 1,000,000 Bytes, 1GB = 1,000,000,000 Bytes, Unformatted Capacity. User accessible capacity may vary depending on operating environment and formatting.
2) 1 Sector = 512Bytes, Max. LBA represents the total user addressable sectors in LBA mode and calculated by IDEMA rule
3) Actual performance may vary depending on use conditions and environment.
4) Measured by SMART Temperature. Proper airflow recommended
5) Active power is measured on sequential write and read.
6) Idle Power is measured on Idle status with L0+APST on.

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1.0 INTRODUCTION

1.1 General Description

This document describes the specification of PM961 SSD which uses PCIe interface.
The PM961 is fully consist of semiconductor device and using NAND Flash Memory which has a high reliability and a high technology in a small form factor for using a SSD and supporting Peripheral Component Interconnect Express (PCIe) 3.0 interface standard up to 4 lanes shows much faster performance than previous SATA SSDs.
The PM961 provides 128GB, 256GB, 512GB and 1TB capacities. It's sequential performance is up to 3000MB/s for read operation and 1700MB/s for write operation by 4 lanes. It's random performance is up to 360k IOPS for read and 330k IOPS for write operation by 4 lanes. It could also provide rugged features with an extreme environment with a high MTBF.

1.2 Product List

[Table 1] Product Line-up

Type	Capacity	Part Number
M.2	128GB	MZVLW128HEGR-00000/07
	256GB	MZVLW256HEHP-00000/07
	512GB	MZVLW512HMJP-00000/07
	1TB	MZVLW1T0HMLH-00000/07

1.3 Ordering Information

M Z X X X X X X X X X X - X X X X X

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18

1. Memory (M)

2. Module Classification
Z: SSD

3. Form Factor
V: PCIeM.2 (22*80)

4. Line-Up
L: VT: Client/SV (VNAND 3bit MLC)

5. SSD CTRL
W: Polaris

6~8. SSD Density
128: 128GB
256: 256GB
512: 512GB
1T0: 1TB

9. NAND PKG + NAND Voltage
H: BGA (LF,HF)

10. Flash Generation
M: 1st Generation
E: 6th Generation

11~12. NAND Density
GR: 512G QDP 4CE
HP: 1T ODP 8CE
JP: 2T ODP 8CE
LH: 4T HDP 16CE

13. "-"

14. Default
"0"

15. HW revision
0: No revision

16. Packaging type
0: Bulk

17~18. Customer
00: General
07: General SED

2.0 PRODUCT SPECIFICATION

2.1 Capacity

[Table 2] User Addressable Sectors

Capacity	Max LBA
128GB[1)]	250,069,680
256GB[1)]	500,118,192
512GB[1)]	1,000,215,216
1TB	2,000,409,264

NOTE:
1) Gigabyte (GB) = 1,000,000,000 Bytes, 1 Sector = 512Bytes
2) Max. LBA shown in Table 1 represents the total user addressable sectors in LBA mode and calculated by IDEMA rule.

2.2 Performance[1)]

[Table 3] Drive Performance

Gen3

Parameter	Unit	Queue Depth	128GB	256GB	512GB	1TB
Sequential Read[2)] (Up to)	MB/s	QD = 32	2800	2800	2800	3000
Sequential Write[2)] (Up to)	MB/s	QD = 32	600	1100	1600	1700
Random Read[3)] (Up to)	IOPS	QD = 1	10K	10K	12K	12K
	IOPS	QD = 32	140K	250K	260K	360K
Random Write[3)] (Up to)	IOPS	QD = 1	40K	50K	50K	50K
	IOPS	QD = 32	40K	180K	260K	330K

NOTE:
1) Performance measured using CDM 5.0.2 on Windows 8.1 64bit. Actual performance may vary depending on use conditions and environment
2) Sequential performance measured using 128KB data size. (QD=32 by Thread=1)
3) Random performance measured using 4KB data size. (QD=32 by Thread 4, QD=1 by Thread 1)
4) Performance measurements based on TurboWrite technology

2.3 Power

[Table 4] Maximum Ratings

Parameter		Specifications
Supply Voltage	Allowable voltage	3.3V ± 5%
	Allowable noise/ripple	100mV p-p or less

[Table 5] Power Consumption for M.2 (3.3V Supply)

Parameter			Specifications
Power Consumption	Active[1] (Typical, RMS)	Read	6.1W
		Write	5.1W
	Idle[2] (Typical)		450mW
	L1.2[3] (Typical)		5mW

NOTE:
1) Active power is measured on sequential write and read.
2) Idle Power is measured on Idle status with L0+APST on.
3) If L1.2 time logging option is enabled, L1.2 Power could be 5mW.

2.4 Reliability

This chapter provides the information for the reliability features of the SSD.

2.4.1 MTBF

MTBF is Mean Time Between Failure, and is the predicted elapsed time between inherent failures of a system during operation. As same word, AFR (annual failure ratio) is 0.4%. MTBF can be calculated as the arithmetic average time between failures of a system.

[Table 6] MTBF Specifications

Capacity	MTBF
128GB	1,500,000 Hours
256GB	
512GB	
1TB	

2.4.2 UBER

UBER is Uncorrectable Bit Error Rate.

[Table 7] UBER Specifications

Parameter	Specification
UBER	< 1 sector per 10^{15} bits read

2.5 Environmental Specification

[Table 8] Temperature, Humidity, Shock, Vibration

Parameter	Mode	Specification
Temperature (Tc)	Operating[1)]	0°C to 70°C
	Non-operating	-40°C to 85°C
Humidity[2)]	Non-operating	5% to 95%
Shock[3)]	Non-operating	1500G
Vibration[4)]	Non-operating	20G

NOTE:
1) Temperature is measured by SMART Temperature. Proper airflow recommended
2) Humidity is measured in non-condensing
3) Test condition for shock: 0.5ms duration with half sine wave
4) Test condition for vibration: 10Hz to 2000Hz

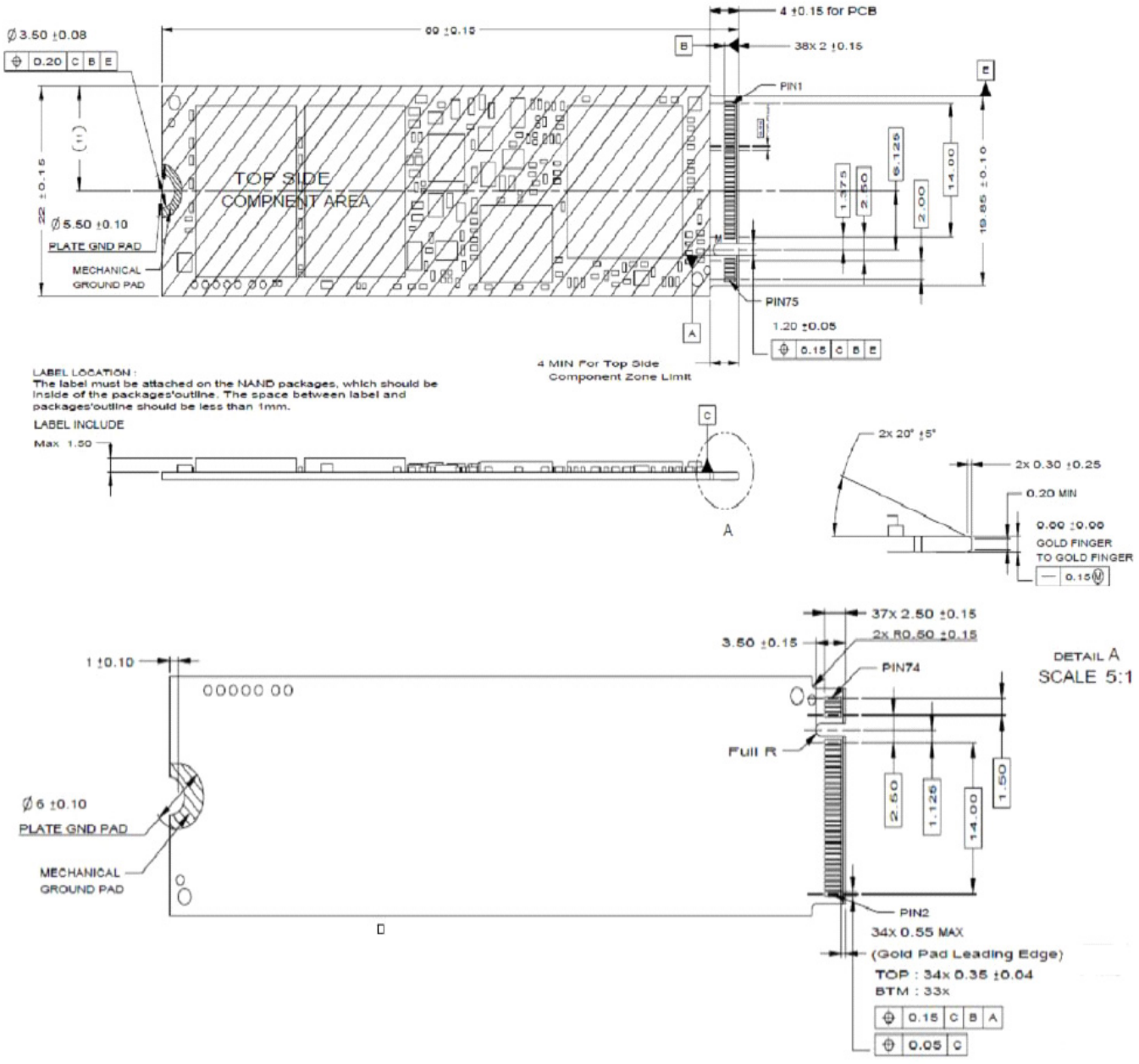
3.0 MECHANICAL SPECIFICATION

3.1 Physical dimensions and Weight

[Table 9] Physical dimensions and Weight

Parameter		Value
Width		22.00 ± 0.15 mm
Length		80.00 ± 0.15 mm
Thickness		Max. 2.38 mm
Weight	128/256/512GB/1TB	Max 8g

3.2 Form Factor

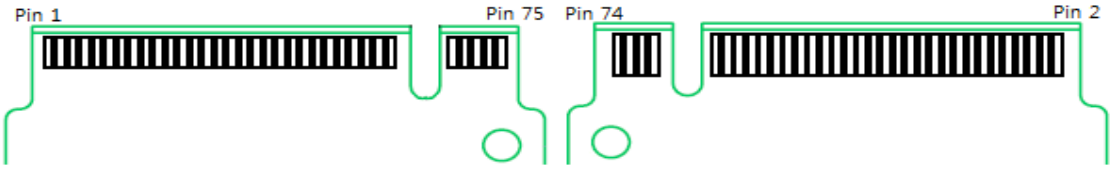


[Figure 1] M.2 Package

4.0 INTERFACE SPECIFACION

4.1 Connector Dimension and Pin Location

[TOP VIEW] [BOTTOM VIEW]



[Figure 2] M.2 Signal and Power pins

4.2 Pin Assignments and Definition

[Table 10] Signal Assignments

Pin#	Assignment	Description	Pin#	Assignment	Description
1	GND	Return current path	2	3.3V	3.3V source
3	GND	Return current path	4	3.3V	3.3V source
5	PETn3	PCIe TX	6	N/C	N/C
7	PETp3	PCIe TX	8	N/C	N/C
9	GND	Return current path	10	LED1#[1)]	Device Active Signal (Refer to [Table 11])
11	PERn3	PCIe Rx	12	3.3V	3.3V source
13	PERp3	PCIe Rx	14	3.3V	3.3V source
15	GND	Return current path	16	3.3V	3.3V source
17	PETn2	PCIe TX	18	3.3V	3.3V source
19	PETp2	PCIe TX	20	N/C	N/C
21	GND	Return current path	22	N/C	N/C
23	PERn2	PCIe Rx	24	N/C	N/C
25	PERp2	PCIe Rx	26	N/C	N/C
27	GND	Return current path	28	N/C	N/C
29	PETn1	PCIe TX	30	N/C	N/C
31	PETp1	PCIe TX	32	N/C	N/C
33	GND	Return current path	34	N/C	N/C
35	PERn1	PCIe Rx	36	N/C	N/C
37	PERp1	PCIe Rx	38	N/C	N/C
39	GND	Return current path	40	N/C	N/C
41	PETn0	PCIe TX	42	N/C	N/C
43	PETp0	PCIe TX	44	N/C	N/C
45	GND	Return current path	46	N/C	N/C
47	PERn0	PCIe Rx	48	N/C	N/C
49	PERp0	PCIe Rx	50	PERST#	PCIe Reset
51	GND	Return current path	52	CLKREQ#	PCIe Device Clock Request
53	REFCLKN	PCIe Reference Clock	54	PEWake#	N/C
55	REFCLKP	PCIe Reference Clock	56	Reserved for MFG_Data	N/C
57	GND	Return current path	58	Reserved for MFG_CLOCK	N/C
67	N/C	N/C	68	SUSCLK	N/C
69	PEDET	N/C	70	3.3V	3.3V source
71	GND	Return current path	72	3.3V	3.3V source
73	GND	Return current path	74	3.3V	3.3V source
75	GND	Return current path			

[Table 11] Simple Indicator Protocol for SSD LED States (Optional)

		LED Status
Active State (Host send CMD to SSD)		Blinking
Idle	Low Power standby	OFF
State	Deep Sleep Power savings	OFF

5.0 PCI and NVM Express registers

5.1 PCI Express Registers

5.1.1 PCI Register Summary

[Table 12] PCI Register Summary

Start Address	End Address	Name	Type
00h	3Fh	PCI Header	PCI Capability
40h	47h	PCI Power Management Capability	PCI Capability
50h	67h	MSI Capability	PCI Capability
70h	A3h	PCI Express Capability	PCI Capability
B0h	BBh	MSI-X Capability	PCI Capability
100h	12Bh	Advanced Error Reporting Capability	PCI Capability
148h	153h	Device Serial No Capability	PCI Capability
158h	167h	Power Budgeting Capability	PCI Capability
168h	177h	Secondary PCI Express Header	PCI Capability
188h	18Fh	Latency Tolerance Reporting (LTR)	PCI Capability
190h	19Fh	L1 Substates Capability Register	PCI Capability

5.1.2 PCI Header Registers

[Table 13] PCI Header Register Summary

Start Address	End Address	Symbol	Description
00h	03h	ID	Identifiers
04h	05h	CMD	Command Register
06h	07h	STS	Device Status
08h	08h	RID	Revision ID
09h	0Bh	CC	Class Codes
0Ch	0Ch	CLS	Cache Line Size
0Dh	0Dh	MLT	Master Latency Timer
0Eh	0Eh	HTYPE	Header Type
0Fh	0Fh	BIST	Built in Self Test
10h	13h	MLBAR (BAR0)	Memory Register Base Address (lower 32-bit)
14h	17h	MUBAR (BAR1)	Memory Register Base Address (upper 32-bit)
18h	1Bh	IDBAR (BAR2)	Index/Data Pair Register Base Address
1Ch	1Fh	BAR3	Reserved
20h	23h	BAR4	Reserved
24h	27h	BAR5	Reserved
28h	2Bh	CCPTR	CardBus CIS Pointer
2Ch	2Fh	SS	Subsystem Identifiers
30h	33h	EROM	Expansion ROM Base Address
34h	34h	CAP	Capabilities Pointer
35h	3Bh	R	Reserved
3Ch	3Dh	INTR	Interrupt Information
3Eh	3Eh	MGNT	Minimum Grant
3Fh	3Fh	MLAT	Maximum Latency

[Table 14] Identifier Register

Bits	Type	Default Value	Description
31:16	RO	A804h	Device ID
0:15	RO	144Dh	Vendor ID

[Table 15] Command Register

Bits	Type	Default Value	Description
15:11	RO	0	Reserved
10	RW	0	Interrupt Disable
9	RO	0	Fast Back-to-Back Enable (N/A)
8	RW	0	SERR# Enable (N/A)
7	RO	0	IDSEL Stepping/Wait Cycle Control (N/A)
6	RW	0	Parity Error Response Enable
5	RO	0	VGA Palette Snooping Enable (N/A)
4	RO	0	Memory Write and Invalidate Enable (N/A)
3	RO	0	Special Cycle Enable (N/A)
2	RW	0	Bus Master Enable
1	RW	0	Memory Space Enable
0	RW	0	I/O Space Enable

[Table 16] Device Status Register

Bits	Type	Default Value	Description
15	RW1C	0	Detected Parity Error
14	RW1C	0	Signaled System Error (N/A)
13	RW1C	0	Received Master Abort
12	RW1C	0	Received Target Abort
11	RW1C	0	Signaled Target Abort (N/A)
10:9	RO	0	DEVSEL Timing (N/A)
8	RW1C	0	Master Data Parity Error Detected
7	RO	0	Fast Back-to-Back Transaction Capable (N/A)
6	RO	0	Reserved
5	RO	0	66MHz Capable (N/A)
4	RO	1	Capabilities List
3	RO	0	INTx Status
2:0	RO	0	Reserved

[Table 17] Revision ID Register

Bits	Type	Default Value	Description
7:0	RO	00h	Controller Hardware Revision ID

[Table 18] Class Code Register

Bits	Type	Default Value	Description
23:16	RO	1h	Base Class Code
15:8	RO	8h	Sub Class Code
7:0	RO	2h	Programming Interface

[Table 19] Cache Line Size Register

Bits	Type	Default Value	Description
7:0	RW	0h	N/A

[Table 20] Master Latency Timer Register

Bits	Type	Default Value	Description
7:0	RO	0	N/A

[Table 21] Header Type Register

Bits	Type	Default Value	Description
7:0	RO	0	N/A

[Table 22] Built In Self Test Register

Bits	Type	Default Value	Description
7:0	RO	0	N/A

[Table 23] Memory Register Base Address Lower 32-bits (BAR0) Register

Bits	Type	Default Value	Description
31:14	RW	0	Base Address
13:4	RO	0	
2:1	RO	2	Address Type (64-bit)
0	RO	0	Memory Space Indicator (MEMSI)

[Table 24] Memory Register Base Address Upper 32-bits (BAR1)

Bits	Type	Default Value	Description
31:0	RO	0	Base Address

[Table 25] Index/Data Pair Register Base Address (BAR2) Register

Bits	Type	Default Value	Description
31:0	RO	0	N/A

[Table 26] BAR3 Register

Bits	Type	Default Value	Description
31:0	RO	0	N/A

[Table 27] Vendor Specific BAR4 Register

Bits	Type	Default Value	Description
31:0	RO	0	N/A

[Table 28] Vendor Specific BAR5 Register

Bits	Type	Default Value	Description
31:0	RO	0	N/A

[Table 29] Cardbus CIS Pointer Register

Bits	Type	Default Value	Description
31:0	RO	0	N/A

[Table 30] Subsystem Identifier Register

Bits	Type	Default Value	Description
31:16	RO	A801	Subsystem ID
15:0	RO	144D	Subsystem Vendor ID

[Table 31] Expansion ROM Register

Bits	Type	Default Value	Description
31:17	RW	0	Expansion ROM Base Address
16:1	RO	0	
0	RW	0	Expansion ROM Enable/Disable

[Table 32] Capabilities Pointer Register

Bits	Type	Default Value	Description
7:0	RO	40h	Capability Pointer (Points to PCI Power Management Capability Offset)

[Table 33] Interrupt Information Register

Bits	Type	Default Value	Description
15:8	RO	01	Interrupt Pin
7:0	RW	FF	Interrupt Line

[Table 34] Minimum Grant Register

Bits	Type	Default Value	Description
7:0	RO	0	Minimum Grant

[Table 35] Maximum Latency Register

Bits	Type	Default Value	Description
7:0	RO	0	Maximum Latency

5.1.3 PCI Power Management Registers

[Table 36] PCI Power Management Capability Register Summary

Start Address	End Address	Symbol	Description
40h	40h	PID	PCI Power Management Capability ID
41h	41h	Next cap ptr	Next cap ptr
42h	43h	PMC	PC Power Management Capabilities
44h	45h	PMCS	PCI Power Management Control and Status
46h	46h	PMCSR_BSE	PMCSR_BSE Bridge Extensions
47h	47h	Data	Data

[Table 37] PCI Power Management Capability ID Register

Bits	Type	Default Value	Description
15:8	RO	50h	Next Capability
7:0	RO	1h	Capability ID

[Table 38] PCI Power Management Capability Register

Bits	Type	Default Value	Description
15:11	RO	0	PME Support (N/A)
10	RO	0	D2 Support
9	RO	0	D1 Support
8:6	RO	0	AUX Current (N/A)
5	RO	0	Device Specific Initialization
4	RsvdP	0	Reserved
3	RO	0	PME Clock
2:0	RO	3h	Version (Support for revision 1.2)

[Table 39] PCI Power Management Control and Status Register

Bits	Type	Default Value	Description
31:24	RsvdP	0	data register
23	RO	0	Bus power/Clock enable
22	RO	0	B2, B3 support
21:16	RsvdP	0	Reserved
15	RO	0	PME_Status (N/A)
14:13	RO	0	Data Scale (N/A)
12:9	RO	0	Data Select (N/A)
8	RWS	0	PME enable (N/A)
7:4	RsvdP	0	Reserved
3	RO	1	No Soft Reset
2	RsvdP	0	Reserved
1:0	RW	0	Power State

5.1.4 Message Signaled Interrupt Registers

[Table 40] Message Signaled Interrupt Capability Register Summary

Start Address	End Address	Symbol	Description
50h	51h	MID	Message Signaled Interrupt Capability ID
52h	53h	MC	Message Signaled Interrupt Message Control
54h	57h	MA	Message Signaled Interrupt Message Address
58h	5Bh	MUA	Message Signaled Interrupt Upper Address
5Ch	5Dh	MD	Message Signaled Interrupt Message Data
60h	63h	MMASK	Message Signaled Interrupt Mask Bits
64h	67h	MPEND	Message Signaled Interrupt Pending Bits

[Table 41] Message Signaled Interrupt Capability ID Register

Bits	Type	Default Value	Description
15:8	RO	70h	Next Capability
7:0	RO	05h	Capability ID

[Table 42] Message Signaled Interrupt Control Register

Bits	Type	Default Value	Description
15:9	RsvdP	0	Reserved
8	RO	0	Per Vector Masking Capable
7	RO	1h	64-bit Address Capable
6:4	RW	0h	Multiple Message Enable
3:1	RO	5h	Multiple Message Capable
0	RW	0h	MSI Enable

[Table 43] Message Signaled Interrupt Address Register

Bits	Type	Default Value	Description
31:2	RW	0	Address
1:0	RO	0	Reserved

[Table 44] Message Signaled Interrupt Upper Address Register

Bits	Type	Default Value	Description
31:0	RW	0	Upper Address

[Table 45] Message Signaled Interrupt Message Data Register

Bits	Type	Default Value	Description
16:31	RsvdP	0	Reserved
0:15	RO	0	Data

[Table 46] Message Signaled Interrupt Mask Bits Register

Bits	Type	Default Value	Description
31:0	RW	0	Mask Bits

[Table 47] Message Signaled Interrupt Pending Bits Register

Bits	Type	Default Value	Description
31:0	RO	0	Pending Bits

5.1.5 MSI-X Registers

[Table 48] MSI-X Capability Register Summary

Start Address	End Address	Symbol	Description
B0h	B1h	MXID	MSI-X Capability ID
B2h	B3h	MXC	MSI-X Message Control
B4h	B7h	MTAB	MSI-X Table Offset and Table BIR
B8h	BBh	MPBA	MSI-X PBA Offset and PBA BIR

[Table 49] MSI-X Identifier Register

Bits	Type	Default Value	Description
15:8	RO	00h	Next Capability
7:0	RO	11h	Capability ID

[Table 50] MSI-X Control Register

Bits	Type	Default Value	Description
15	RW	0	MSI-X Enable
14	RW	0	Function Mask
13:11	RsvdP	0	Reserved
10:0	RO	20h	Table Size

[Table 51] MSI-X Table Offset Register

Bits	Type	Default Value	Description
31:3	RO	600h	Table Offset
2:0	RO	0	Table BIR

[Table 52] MSI-X Pending Bit Array Offset Register

Bits	Type	Default Value	Description
31:3	RO	400h	Pending Bit Array Offset
2:0	RO	0	Pending Bit Array BIR

5.1.6 PCI Express Capability Registers

[Table 53] PCI Express Capability Register Summary

Start Address	End Address	Symbol	Description
70h	71h	PXID	PCI Express Capability ID
72h	73h	PXCAP	PCI Express Capabilities
74h	77h	PXDCAP	PCI Express Device Capabilities
78h	79h	PXDC	PCI Express Device Control
7Ah	7Bh	PXDS	PCI Express Device Status
7Ch	7Fh	PXLCAP	PCI Express Link Capabilities
80h	81h	PXLC	PCI Express Link Control
82h	83h	PXLS	PCI Express Link Status
94h	97h	PXDCAP2	PCI Express Device Capabilities 2
98h	99h	PXDC2	PCI Express Device Control 2
9Ah	9Bh	PXDS2	PCI Express Device Status 2
9Ch	9Fh	PXLCAP2	PCI Express Link Capabilities 2
A0h	A1h	PXLC2	PCI Express Link Control 2
A2h	A3h	PXLS2	PCI Express Link Status 2

[Table 54] PCI Express Capability ID Register

Bits	Type	Default Value	Description
15:8	RO	B0h	Next Pointer (MSI-X Capability)
7:0	RO	10h	Capability ID

[Table 55] PCI Express Capabilities Register

Bits	Type	Default Value	Description
15:14	RsvdP	0	Reserved
13:9	RO	0	Interrupt Message Number
8	HwInit	0	Slot Implementation (N/A)
7:4	RO	0	Device/Port Type
3:0	RO	2h	Capability Version

[Table 56] PCI Express Device Capabilities Register

Bits	Type	Default Value	Description
31:29	RsvdP	0	Reserved
28	RO	1	Function Level Reset Capability
27:26	RO	0	Captured Slot Power Limit Scale
25:18	RO	0	Captured Slot Power Limit Value
17:16	RsvdP	0	Reserved
15	RO	1	Role-based Error Reporting
14:12	RO	0	Reserved
11:9	RO	7h	Endpoint L1 Acceptable Latency
8:6	RO	7h	Endpoint L0 Acceptable Latency
5	RO	0	Extended Tag Field Supported
4:3	RO	0	Phantom Functions Supported
2:0	RO	1h	Max Payload Size Supported (256 byte payload)

[Table 57] PCI Express Device Control Register

Bits	Type	Default Value	Description
15	RW	0	Initiate Function Level Reset
14:12	RW	2h	Max Read Request Size
11	RW	1	Enable No Snoop
10	RWS	0	Aux Power PM Enable (N/A)
9	RW	0	Phantom Functions Enable (N/A)
8	RW	0	Extended Tag Enable
7:5	RW	0	Max Payload Size
4	RW	1	Enable Relaxed Ordering (N/A)
3	RW	0	Unsupported Request Reporting Enable
2	RW	0	Fatal Error Reporting Enable
1	RW	0	Non-Fatal Error Reporting Enable
0	RW	0	Correctable Error Reporting Enable

[Table 58] PCI Express Device Status Register

Bits	Type	Default Value	Description
15:6	RsvdZ	0	Reserved
5	RO	0	Transactions Pending
4	RO	1	Aux Power Detected
3	RW1C	0	Unsupported Request Detected
2	RW1C	0	Fatal Error Detected
1	RW1C	0	Non-Fatal Error Detected
0	RW1C	0	Correctable Error Detected

[Table 59] PCI Express Link Capabilities Register

Bits	Type	Default Value	Description
31:24	HwInit	0 (Port 0)	Port Number
23	RsvdP	0	Reserved
22	HwInit	1h	ASPM Optionality Compliance
21	RO	0	Link Bandwidth Notification Capability (N/A)
20	RO	0	Data Link Layer Link Active Reporting Capable (N/A)
19	RO	0	Surprise Down Error Reporting Capable (N/A)
18	RO	1	Clock Power Management
17:15	RO	6	L1 Exit Latency
14:12	RO	7h	L0s Exit Latency
11:10	RO	2	Active State Power Management Support
9:4	RO	4h (x4 link)	Maximum Link Width
3:0	RO	3h	Supported Link Speeds

[Table 60] PCI Express Link Control Register

Bits	Type	Default Value	Description
15:12	RsvdP	0	Reserved
11	RsvdP	0	Link Autonomous Bandwidth Interrupt Enable
10	RsvdP	0	Link Bandwidth Management Interrupt Enable
9	RsvdP	0	Hardware Autonomous Width Disable
8	RW	0	Enable Clock Power Management
7	RW	0	Extended Sync
6	RW	0	Common Clock Configuration
5	RsvdP	0	Retrain Link
4	RsvdP	0	Link Disable
3	Root Ports (RO) End Points & Bridges (RW) Switch Ports (RO)	0	Read Completion Boundary (N/A)
2	RsvdP	0	Reserved
1:0	RW	0	Active State Power Management Control

[Table 61] PCI Express Link Status Register

Bits	Type	Default Value	Description
15	RW1C	0	Link Autonomous Bandwidth Status
14	RW1C	0	Link Bandwidth Management Status
13	RO	0	Data Link Layer Link Active
12	HwInit	1	Slot Clock Configuration
11	RO	0	Link Training (1: Link training in progress;0: No link training in progress) (Non-standard)
10	RO	0	Reserved
9:4	RO	1	Negotiated Link Width
3:0	RO	1	Current Link Speed

[Table 62] PCI Express Device Capabilities 2 Register

Bits	Type	Default Value	Description
31	HwInit	0	FRS Supported (N/A)
30:24	RsvdP	0	Reserved
23:22	HwInit	0	Max End-End TLP Prefixes (N/A)
21	HwInit	0	End-End TLP Prefix Supported (N/A)
20	RO	0	Extended Format Field Supported (N/A)
19:18	HwInit	0	OBFF Supported (N/A)
17:16	RsvdP	0	Reserved
15:14	HwInit	0	LN System CLS (N/A)
13:12	RO	0	TPH Completer Supported (N/A)
11	RO	1	Latency Tolerance Reporting Supported (N/A)
10	HwInit	0	No RO-enabled PR-PR Passing (N/A)
9	RO	0	128-bit CAS Completer Supported (N/A)
8	RO	0	64-bit Atomic Op Completer Supported (N/A)
7	RO	0	32-bit Atomic Op Completer Supported (N/A)
6	RO	0	Atomic Op Routing Supported (N/A)
5	RO	0	ARI Forwarding Supported (N/A)
4	RO	1	Completion Timeout Disable Supported
3:0	HwInit	Fh	Completion Timeout Ranges Supported (50us to 200ms)

[Table 63] PCI Express Device Control 2 Register

Bits	Type	Default Value	Description
15	RsvdP	0	End-to-end TLP Prefix Blocking (N/A)
14:13	RW/RsvdP	0	OBFF Enable (N/A)
12:11	RsvdP	0	Reserved
10	RW/RsvdP	0	Latency Tolerance Reporting Mechanism Enable (N/A)
9	RW	0	IDO Completion Enable
8	RW	0	IDO Request Enable
7	RW	0	AtomicOp Egress Blocking
6	RW	0	AtomicOp Requester Enable
5	RW	0	ARI Forwarding Enable
4	RW	0	Completion Timeout Disable
3:0	RW	0	Completion Timeout Value (0h - 50 µs; 1h - 100 µs; 2h - 2 ms; 5h - 50 ms; 6h - 200 ms; others - reserved)

[Table 64] PCI Express Device Status 2 Register

Bits	Type	Default Value	Description
15:0	RsvdZ	0	Reserved

[Table 65] PCI Express Link Capabilities 2 Register

Bits	Type	Default Value	Description
31:9	RsvdP	0	Reserved
8	RO	0	Cross-Link Supported (N/A)
7:1	RO	7h	Supported Link Speeds 001b: 2.5 GT/s (Gen 1) 010b: 5.0 GT/s (Gen 2) 100b: 8 GT/s (Gen 3)
0	RsvdP	0	Reserved

[Table 66] PCI Express Link Control 2 Register

Bits	Type	Default Value	Description
15:12	RWS/RsvdP	0	Compliance De-emphasis
11	RWS/RsvdP	0	Compliance SOS
10	RWS/RsvdP	0	Enter Modified Compliance
9:7	RWS/RsvdP	0	Transmit Margin
6	HwInit	0	Select De-Emphasis
5	RWS/RsvdP	0	Hardware Autonomous Speed Disable
4	RWS/RsvdP	0	Enter Compliance
3:0	RWS/RsvdP	3h	Target Link Speed 1h: 2.5 GT/s (Gen 1) 2h: 5.0 GT/s (Gen 2) 3h: 8 GT/s (Gen 3)

[Table 67] PCI Express Link Status 2 Register

Bits	Type	Default Value	Description
15:6	RsvdZ	0	Reserved
5	RW1CS	0	Link Equalization Request
4	ROS	0	Equalization Phase 3 Successful
3	ROS	0	Equalization Phase 2 Successful
2	ROS	0	Equalization Phase 1 Successful
1	ROS	0	Equalization Complete
0	RO	1	Current De-Emphasis

5.1.7 Advanced Error Reporting Registers

[Table 68] Advanced Error Reporting Capability Register Summary

Start Address	End Address	Symbol	Description
100h	103h	AERID	AER Capability ID
104h	107h	AERUCES	AER Uncorrectable Error Status
108h	10Bh	AERUCEM	AER Uncorrectable Error Mask
10Ch	10Fh	AERUCESEV	AER Uncorrectable Error Severity
110h	113h	AERCES	AER Correctable Error Status
114h	117h	AERCEM	AER Correctable Error Mask
118h	11Bh	AERCC	AER Advanced Error Capabilities and Control
11Ch	12Bh	AERHL	AER Header Log

[Table 69] AER Capability ID Register

Bits	Type	Default Value	Description
31:20	RO	148h	Next Pointer (Points to Secondary PCI Express Extended Capability Header Offset)
19:16	RO	2h	Capability Version
15:0	RO	1h	Capability ID

[Table 70] AER Uncorrectable Error Status Register

Bits	Type	Default Value	Description
31:27	RsvdZ	0	Reserved
26	RW1CS	0	Poisoned TLP Egress Blocked Status (N/A)
25	RW1CS	0	TLP Prefix Blocked Error Status (N/A)
24	RW1CS	0	Atomic Op Egress Blocked Status (N/A)
23	RW1CS	0	MC Blocked TLP Status (N/A)
22	RW1CS	0	Uncorrectable Internal Error Status (N/A)
21	RW1CS	0	ACS Violation Status (N/A)
20	RW1CS	0	Unsupported Request Error Status
19	RW1CS	0	ECRC Error Status
18	RW1CS	0	Malformed TLP Status
17	RW1CS	0	Receiver Overflow Status
16	RW1CS	0	Unexpected Completion Status
15	RW1CS	0	Completer Abort Status
14	RW1CS	0	Completion Timeout Status
13	RW1CS	0	Flow Control Protocol Error Status
12	RW1CS	0	Poisoned TLP Status
11:6	RsvdZ	0	Reserved
5	RW1CS	0	Surprise Down Error Status (N/A)
4	RW1CS	0	Data Link Protocol Error Status
3:1	RsvdZ	0	Reserved
0	Undefined	0	Undefined

[Table 71] AER Uncorrectable Error Mask Register

Bits	Type	Default Value	Description
31:27	RsvdZ	0	Reserved
26	RWS	0	Poisoned TLP Egress Blocked Mask (N/A)
25	RWS	0	TLP Prefix Blocked Error Mask (N/A)
24	RWS	0	Atomic Op Egress Blocked Mask (N/A)
23	RWS	0	MC Blocked TLP Mask (N/A)
22	RWS	1	Uncorrectable Internal Error Mask (N/A)
21	RWS	0	ACS Violation Mask (N/A)
20	RWS	0	Unsupported Request Error Mask
19	RWS	0	ECRC Error Mask
18	RWS	0	Malformed TLP Mask
17	RWS	0	Receiver Overflow Mask
16	RWS	0	Unexpected Completion Mask
15	RWS	0	Completer Abort Mask
14	RWS	0	Completion Timeout Mask
13	RWS	0	Flow Control Protocol Error Mask
12	RWS	0	Poisoned TLP Mask
11:6	RsvdZ	0	Reserved
5	RWS	0	Surprise Down Error Mask (N/A)
4	RWS	0	Data Link Protocol Error Mask
3:1	RsvdZ	0	Reserved
0	Undefined	0	Undefined

[Table 72] AER Uncorrectable Error Severity Register

Bits	Type	Default Value	Description
31:27	RsvdP	0	Reserved
26	RWS	0	Poisoned TLP Egress Blocked Severity (N/A)
25	RWS	0	TLP Prefix Blocked Error Severity (N/A)
24	RWS	0	Atomic Op Egress Blocked Severity (N/A)
23	RWS	0	MC Blocked TLP Severity (N/A)
22	RWS	1	Uncorrectable Internal Error Severity (N/A)
21	RWS	0	ACS Violation Severity (N/A)
20	RWS	0	Unsupported Request Error Severity
19	RWS	0	ECRC Error Severity
18	RWS	1	Malformed TLP Severity
17	RWS	1	Receiver Overflow Severity
16	RWS	0	Unexpected Completion Severity
15	RWS	0	Completer Abort Severity
14	RWS	0	Completion Timeout Severity
13	RWS	1	Flow Control Protocol Error Severity
12	RWS	0	Poisoned TLP Severity
11:6	RsvdP	0	Reserved
5	RWS	1	Surprise Down Error Severity (N/A)
4	RWS	1	Data Link Protocol Error Severity
3:1	RsvdP	0	Reserved
0	Undefined	0	Undefined

[Table 73] AER Correctable Error Status Register

Bits	Type	Default Value	Description
31:16	RsvdZ	0	Reserved
15	RW1CS	0	Header Log Overflow Status (N/A)
14	RW1CS	0	Corrected Internal Error Status (N/A)
13	RW1CS	0	Advisory Non-Fatal Error Status
12	RW1CS	0	Replay Timer Timeout Status
11:9	RsvdZ	0	Reserved
8	RW1CS	0	Replay Number Rollover Status
7	RW1CS	0	Bad DLLP Status
6	RW1CS	0	Bad TLP Status
5:1	RsvdZ	0	Reserved
0	RW1CS	0	Received Error Status

[Table 74] AER Correctable Error Mask Register

Bits	Type	Default Value	Description
31:16	RsvdP	0	Reserved
15	RWS	0	Header Log Overflow Mask (N/A)
14	RWS	1	Corrected Internal Error Mask (N/A)
13	RWS	1	Advisory Non-Fatal Error Mask
12	RWS	0	Replay Timer Timeout Mask
11:9	RsvdP	0	Reserved
8	RWS	0	Replay Number Rollover Mask
7	RWS	0	Bad DLLP Mask
6	RWS	0	Bad TLP Mask
5:1	RsvdP	0	Reserved
0	RWS	0	Received Error Mask

[Table 75] AER Capabilities and Control Register

Bits	Type	Default Value	Description
31:13	RsvdP	0	Reserved
12	RO	0	Completion Timeout Prefix/Header Log Capable (N/A)
11	ROS	0	TLP Prefix Log Present (N/A)
10	RWS	0	Multiple Header Recording Enable (N/A)
9	RO	0	Multiple Header Recording Capable (N/A)
8	RWS	0	ECRC Check Enable
7	RO	1	ECRC Check Capable
6	RWS	0	ECRC Generation Enable
5	RO	1	ECRC Generation Capable
4:0	ROS	0	First Error Pointer

[Table 76] AER Header Log Register

Bits	Type	Default Value	Description
127:120	ROS	0	Header Byte 0
119:112	ROS	0	Header Byte 1
111:104	ROS	0	Header Byte 2
103:96	ROS	0	Header Byte 3
95:88	ROS	0	Header Byte 4
87:80	ROS	0	Header Byte 5
79:72	ROS	0	Header Byte 6
71:64	ROS	0	Header Byte 7
63:56	ROS	0	Header Byte 8
55:48	ROS	0	Header Byte 9
47:40	ROS	0	Header Byte 10
39:32	ROS	0	Header Byte 11
31:24	ROS	0	Header Byte 12
23:16	ROS	0	Header Byte 13
15:8	ROS	0	Header Byte 14
7:0	ROS	0	Header Byte 15

[Table 77] Secondary PCI Express Capability Register Summary

Start Address	End Address	Symbol	Description
168h	16Bh	SPXID	Secondary PCI Express Capability
16Ch	16Fh	PXLC3	PCI Express Link Control 3
170h	173h	PXLE	PCI Express Lane Error Status
174h	175h	PXL0EC	PCI Express Lane 0 Equalization Control
176h	177h	PXL1EC	PCI Express Lane 1 Equalization Control
178h	179h	PXL2EC	PCI Express Lane 2 Equalization Control
17Ah	17Bh	PXL3EC	PCI Express Lane 3 Equalization Control

[Table 78] Secondary PCI Express Capability ID Register

Bits	Type	Default Value	Description
31:20	RO	188h	Next Pointer (Samsung Vendor Specific Capability)
19:16	RO	1h	Capability Version
15:0	RO	0019h	Capability ID (Secondary PCI Express Extended capability)

[Table 79] PCI Express Link Control 3 Register

Bits	Type	Default Value	Description
31:2	Rsvdp	0	Reserved
1	Rsvdp	0	Link Equalization Request Interrupt Enable (N/A)
0	Rsvdp	0	Perform Equalization (N/A)

[Table 80] PCI Express Lane Error Status Register

Bits	Type	Default Value	Description
31:4	Rsvdp	0	Reserved
3:0	RW1CS	0	Lane Error Status Bits

[Table 81] PCI Express Lane 0 Equalization Register

Bits	Type	Default Value	Description
15	RsvdP	0	Reserved
14:12	HwInit/RO	7h	Upstream Port Receiver Preset Hint
11:8	HwInit/RO	Fh	Upstream Port Transmitter Preset
7	RsvdP	0	Reserved
6:4	HwInit/RsvdP	0	Downstream Port Receiver Preset Hint (N/A)
3:0	HwInit/RsvdP	0	Downstream Port Transmitter Preset (N/A)

[Table 82] PCI Express Lane 1 Equalization Register

Bits	Type	Default Value	Description
15	RsvdP	0	Reserved
14:12	HwInit/RO	7h	Upstream Port Receiver Preset Hint
11:8	HwInit/RO	Fh	Upstream Port Transmitter Preset
7	RsvdP	0	Reserved
6:4	HwInit/RsvdP	0	Downstream Port Receiver Preset Hint (N/A)
3:0	HwInit/RsvdP	0	Downstream Port Transmitter Preset (N/A)

[Table 83] PCI Express Lane 2 Equalization Register

Bits	Type	Default Value	Description
15	RsvdP	0	Reserved
14:12	HwInit/RO	7h	Upstream Port Receiver Preset Hint
11:8	HwInit/RO	Fh	Upstream Port Transmitter Preset
7	RdvdP	0	Reserved
6:4	HwInit/RsvdP	0	Downstream Port Receiver Preset Hint (N/A)
3:0	HwInit/RsvdP	0	Downstream Port Transmitter Preset (N/A)

[Table 84] PCI Express Lane 3 Equalization Register

Bits	Type	Default Value	Description
15	RsvdP	0	Reserved
14:12	HwInit/RO	7h	Upstream Port Receiver Preset Hint
11:8	HwInit/RO	Fh	Upstream Port Transmitter Preset
7	RsvdP	0	Reserved
6:4	HwInit/RsvdP	0	Downstream Port Receiver Preset Hint (N/A)
3:0	HwInit/RsvdP	0	Downstream Port Transmitter Preset (N/A)

5.1.8 Device Serial Number Capability Register

[Table 85] Device Serial Number Capability Register Summary

Start Address	End Address	Symbol	Description
148h	14Bh	DSNID	Device Serial Number Capability ID
14Ch	14Fh	SNRL	Serial Number Register (Lower DW)
150h	153h	SNRU	Serial Number Register (Upper DW)

[Table 86] Device Serial Number Capability Register Header

Bits	Type	Default Value	Description
31:20	RO	158h	Next Capability Offset
19:16	HwInit	1h	Capability Version
15:0	HwInit	3h	PCI Express Extended Capability ID

[Table 87] Serial Number Register Header (Lower DW)

Bits	Type	Default Value	Description
31:0	RO	0	Serial Number register (Lower DW)

[Table 88] Serial Number Register Header (Upper DW)

Bits	Type	Default Value	Description
31:0	RO	0	Serial Number register (Upper DW)

5.1.9 Power Budgeting Extended Capability

[Table 89] Power Budgeting Extended Capability Register Summary

Start Address	End Address	Symbol	Description
158h	15Bh	PBXID	Power Budgeting Extended Capability ID
15Ch	15Fh	DSR	Data Select Register
160h	163h	DR	Data Register
164h	167h	PBCR	Power Budget Capability Register

[Table 90] Power Budgeting Extended Capability Header

Bits	Type	Default Value	Description
31:20	RO	168h	Next Capability Offset
19:16	RO	1h	Capability Version
15:00	RO	4h	PCI Express Extended Capability ID

[Table 91] Data Select Register

Bits	Type	Default Value	Description
31:8	RsvdP	0	Reserved
7:0	RW	0	Data Select

[Table 92] Data Register

Bits	Type	Default Value	Description
31:21	RsvdP	0	Reserved
20:18	RO	0	Power Rail
17:15	RO	0	Type
14:13	RO	0	PM State
12:10	RO	0	PM Sub State
9:8	RO	0	Data Scale
7:0	RO	0	Base Power

[Table 93] Power Budget Capability Register

Bits	Type	Default Value	Description
7:1	RsvdP	0	Reserved
0	HwInit	1h	System Allocated

5.1.10 Latency Tolerance Reporting Capability Registers

[Table 94] Latency Tolerance Reporting Capability Register Summary

Start Address	End Address	Symbol	Description
188h	18Bh	LTRID	Latency Tolerance Reporting (LTR) Capability ID
18Ch	18Dh	LTRMNSLR	LTR Max No-Snoop Latency Register
18Eh	18Fh	LTRMSLR	LTR Max Snoop Latency Register

[Table 95] LTR Extended Capability Header

Bits	Type	Default Value	Description
31:20	RO	190h	Next Capability Offset
19:16	RO	1h	Capability Version
15:0	RO	18h	PCI Express Extended Capability ID

[Table 96] LTR Max Snoop latency Register

Bits	Type	Default Value	Description
15:13	RsvdP	0	Reserved
12:10	RW	0	Max Snoop latency Scale
9:0	RW	0	Max Snoop latency Value

[Table 97] LTR Max No Snoop latency Register

Bits	Type	Default Value	Description
15:13	RsvdP	0	Reserved
12:10	RW	0	Max No Snoop Latency Scale
9:0	RW	0	Max No Snoop Latency Value

5.1.11 L1 Substates Capability Registers

[Table 98] L1 Substate Capability Register Summary

Start Address	End Address	Symbol	Description
190h	193h	L1SCID	L1 Substate Capability ID
194h	197h	L1SCR	L1 Substate Capability Register
198h	19Bh	L1SC1R	L1 Substate Control 1 Register
19Ch	19Fh	L1SC2R	L1 Substate Control 2 Register

[Table 99] L1 Substates Extended Capability Header

Bits	Type	Default Value	Description
31:20	RO	0	Next Capability Offset
19:16	RO	1h	Capability Version
15:0	RO	1Eh	PCI Express Extended Capability ID

[Table 100] L1 Substate Capability Register

Bits	Type	Default Value	Description
31:24	RsvdP	0	Reserved
23:19	HwInit	5h	Port Power on value
18	RsvdP	0	Reserved
17:16	HwInit	0	Port T_Power_on scale
15:8	HwInit	Ah	Port Common_mode_restore_time
7:5	RsvdP	0	Reserved
4	HwInit	1	L1 PM Substates Supported
3	HwInit	1	ASPM PM L1.1 Supported
2	HwInit	1	ASPM PM L1.2 Supported
1	HwInit	1	PCI PM L1.1 Supported
0	HwInit	1	PCI PM L1.2 Supported

[Table 101] L1 Substate Control 1 Register

Bits	Type	Default Value	Description
31:29	RW	0	LTR L1.2 Threshold Scale
28:26	RsvdP	0	Reserved
25:16	RW	0	LTR L1.2 Threshold value
15:8	RsvdP	0	Common_mode_restore_time
7:4	RsvdP	0	Reserved
3	RW	0	ASPM PM L1.1 Supported
2	RW	0	ASPM PM L1.2 Supported
1	RW	0	PCI PM L1.1 Supported
0	RW	0	PCI PM L1.2 Supported

[Table 102] L1 Substate Control 2 Register

Bits	Type	Default Value	Description
31:8	RsvdP	0	Reserved
7:3	RW	5	T_POWER_ON Value
2	RsvdP	0	Reserved
1:0	RW	0	T_POWER_ON Scale

5.2 NVM Express Registers

5.2.1 Register Summary

[Table 103] Register Summary

Start Address	End Address	Name	Type
00h	07h	CAP	Controller Capabilities
08h	0Bh	VS	Version
0Ch	0Fh	INTMS	Interrupt Mask Set
10h	13h	INTMC	Interrupt Mask Clear
14h	17h	CC	Controller Configuration
18h	1Bh	Reserved	Reserved
1Ch	1Fh	CSTS	Controller Status
20h	23h	NSSR	NVM Subsystem Reset
24h	27h	AQA	Admin Queue Attributes
28h	2Fh	ASQ	Admin Submission Queue Base Address
30h	37h	ACQ	Admin Completion Queue Base Address
38h	EFFh	Reserved	Reserved
F00h	FFFh	Reserved	Command Set Specific
1000h	1003h	SQ0TDBL	Submission Queue 0 Tail Doorbell (Admin)
1000h + (1 * (4 << CAP.DSTRD))	1003h + (1 * (4 << CAP.DSTRD))	CQ0HDBL	Completion Queue 0 Head Doorbell (Admin)
...			
1000h+ (2y * (4 << CAP.DSTRD))	1003h + (2y * (4 << CAP.DSTRD))	SQyTDBL	Submission Queue y Tail Doorbell
1000h + ((2y + 1) * (4 << CAP.DSTRD))	1003h + ((2y + 1) * (4 << CAP.DSTRD))	CQYHDBL	Completion Queue y Head Doorbell

5.2.2 Controller Registers

[Table 104] Controller Capabilities

Bits	Type	Name	Default Value	Description
63:56	RO		0h	Reserved
55:52	RO	MPSMAX	Fh	Memory Page Size Maximum (Maximum is 128MB)
51:48	RO	MPSMIN	0	Memory Page Size Minimum (Minimum is 4KB)
47:45	RO		0	Reserved
44:37	RO	CSS	1h	Command Sets Supported 1h: NVM command set
36	RO	NSSRS	1h	NVM Subsystem Reset Supported
35:32	RO	DSTRD	0	Doorbell Stride 0: Stride of 4 bytes
31:24	RO	TO	3Ch	Timeout 3Ch: 30 seconds
23:19	RO		0	Reserved
18:17	RO	AMS	1	Arbitration Mechanism Supported (Weighted Round Robin with Urgent supported)
16	RO	CQR	1	Contiguous Queues Required
15:00	RO	MQES	3FFFh	Maximum Queue Entries Supported (16384 entries supported)

[Table 105] Version

Bits	Type	Name	Default Value	Description
31:16	RO	MJR	1h	Major Version Number
15:08	RO	MNR	2h	Minor Version Number
7:00	RO	Reserved	0	Reserved

NOTE:
Note : The PM961 supports NVM Express version 1.2 (Partial)

[Table 106] Interrupt Mask Set

Bits	Type	Name	Default Value	Description
31:00	RW1S	IVMS	0	Interrupt Vector Mask Set

[Table 107] Interrupt Mask Clear

Bits	Type	Name	Default Value	Description
31:00	RW1C	IVMC	0	Interrupt Vector Mask Clear

[Table 108] Controller Configuration

Bits	Type	Name	Default Value	Description
31:24	RO	-	0	Reserved
23:20	RW	IOCQES	0	I/O Completion Queue Entry Size (Configured as a power of 2) (Should be set to 4 for a 16 byte entry size)
19:16	RW	IOSQES	0	I/O Submission Queue Entry Size (Configured as a power of 2) (Should be set to 6 for a 64 byte entry size)
15:14	RW	SHN	0	Shutdown Notification 0h: No notification 1h: Normal shutdown notification 2h: Abrupt shutdown notification 3h: Reserved CSTS.SHST indicates shutdown status.
13:11	RW	AMS	0	Arbitration Mechanism Selected 0h: Round Robin No other values supported.
10:7	RW	MPS	0	Memory Page Size MPS is 2^(12+MPS) Shall be within CAP.MPSMAX and CAP.MPSMIN ranges.
6:4	RW	CSS	0	Command Set Selected 0h: NVM Command Set No other values supported
3:1	RO	-	0	Reserved
0	RW	EN	0	Enable When set to 1, controller shall process commands. When cleared to 0, controller shall not process commands. This field is subject to CSTS.RDY and CAP.TO restrictions.

[Table 109] Controller Status

Bits	Type	Name	Default Value	Description
31:5	RO	-	0	Reserved
4	RW1C	NSSRO	0	NVM Subsystem Reset Occurred
3:2	RO	SHST	0	Shutdown Status 0h: Normal operation, no shutdown requested 1h: Shutdown processing occurring 2h: Shutdown processing complete 3h: Reserved
1	RO	CFS	0	Controller Fatal Status
0	RO	RDY	0	1h: Controller ready to process commands 0h: Controller shall not process commands.

[Table 110] NVM Subsystem Reset

Bits	Type	Name	Default Value	Description
31:0	RW	NSSRC	0	NVM Subsystem Reset Control

[Table 111] Admin Queue Attributes

Bits	Type	Name	Default Value	Description
31:28	RO	-	0	Reserved
27:16	RW	ACQS	0	Admin Completion Queue Size Max: 4096 (Value of 4095h - 0's based value)
15:12	RO	-	0	Reserved
11:0	RW	ASQS	0	Admin Submission Queue Size Max: 4096 (Value of 4095h - 0's based value)

[Table 112] Admin Submission Queue Base Address

Bits	Type	Name	Default Value	Description
63:12	RW	ASQB	0	Admin Submission Queue Base Address
11:0	RO	-	0	Reserved

[Table 113] Admin Completion Queue Base Address

Bits	Type	Name	Default Value	Description
63:12	RW	ACQB	0	Admin Completion Queue Base Address
11:0	RO	-	0	Reserved

[Table 114] Submission Queue Tail y Doorbell

Bits	Type	Name	Default Value	Description
31:16	RO		0	Reserved
15:0	RW	SQT	0	Submission Queue Tail

[Table 115] Completion Queue Head y Doorbell

Bits	Type	Name	Default Value	Description
31:16	RO		0	Reserved
15:0	RW	CQH	0	Completion Queue Head

6.0 Supported Command Set

The Admin command sets and NVM I/O command sets of Samsung SSD PM961 are defined in compliant with NVM Express specification revision 1.2.

6.1 Admin Command Set

The Admin command set is the commands that are submitted to the Admin Submission Queues. The detailed specifications are described in NVM Express specification document.

[Table 116] Opcode for Admin Commands

Opcode (Hex)	Command Name
00h	Delete I/O Submission Queue
01h	Create I/O Submission Queue
02h	Get Log Page
04h	Delete I/O Completion Queue
05h	Create I/O Completion Queue
06h	Identify
08h	Abort
09h	Set Feature
0Ah	Get Feature
0Ch	Asynchronous Event Request
10h	Firmware Activate
11h	Firmware Image Download
80h – BFh	I/O Command Set Specific
C0h – FFh	Vendor Specific

6.1.1 Identify Command

The Identify Command returns the data described below.

[Table 117] Identify Controller Data Structure

Bytes	O/M	Default Value	Description
1:0	M	144Dh	PCI Vendor ID
3:2	M	144Dh	PCI Subsystem Vendor ID
23:4	M	S###N#########	Serial Number (ASCII), #:Variables
63:24	M	128GB: SAMSUNG MZVLW128HEGR-00000 256GB: SAMSUNG MZVLW256HEHP-00000 512GB: SAMSUNG MZVLW512HMJP-00000 1024GB: SAMSUNG MZVLW1T0HMLH-00000	Model Number (ASCII)
71:64	M	CX######	Firmware Revision, #:Variables
72	M	2h	Recommended Arbitration Burst
75:73	M	002538h	IEEE OUI
76	O	0	Controller Multi-Path I/O and Namespace Sharing Capabilities Bit 2: 1h - Controller is associated with an SR-IOV Virtual Function 0h - Controller is associated with a PCI Function. Bit 1: 1h - Device has Two or More controller 0h - Device has One Controller Bit 0: 1h - Device has Two or More physical PCI Express ports 0h - Device has One PCI Express port
77	M	0h	Maximum Data Transfer Size 0h: No restrictions on transfer size
79:78	M	2h	Controller ID (CNTLID)
83:80	M	00010200h	Version
87:84	M	000186A0h	RTD3 Resume Latency
91:88	M	004C4B40h	RTD3 Entry Latency
95:92	M	0h	Optional Asynchronous Events Supported
255:96	M	0h	Reserved
257:256	M	17h	Optional Admin Command Support Bits 15:5 - Reserved Bit 4: 1h - Device Self-Test Bit 3: 0h - Namespace Management Attachment Not Supported Bit 2: 1h – Firmware Activate/Download Supported Bit 1: 1h Format NVM Supported Bit 0: 1h Security Send and Security Receive Supported
258	M	7h	Abort Command Limit (Maximum number of concurrently outstanding Abort commands) (0's based value)
259	M	3h	Asynchronous Event Request Limit (Maximum number of concurrently outstanding Asynchronous Event Request commands) (0's based value)
260	M	16h	Firmware Updates Bits 7:5 – Reserved Bit 4 - 1h Support firmware activation without a reset Bits 3:1 – Number of firmware slots Bit 0 – 0h, "1" indicates Slot 1 is read only
261	M	1h	Log Page Attributes Bits 7:1 – Reserved Bit 0: 1h SMART data is global for all namespaces
262	M	3Fh	Error Log Page Entries (Number of Error Information log entries stored by controller) (0's based value)

263	M	4h	Number of Power States Support (0's based value)
264	M	1h	Admin Vendor Specific Command Configuration Bits 7:1 – reserved Bit 0 – Indicates Admin Vendor Specific Commands use the format defined in NVM Express 1.0c Figure 8.
265	O	1h	Autonomous Power State Transition Attributes (APSTA)
267:266	M	015Eh	Warning Composite Temperature Threshold
269:268	M	0161h	Critical Composite Temperature Threshold
271:270	O	0h	Maximum Time for Firmware Activation
275:272	O	0h	Host Memory Buffer Preferred Size
279:276	O	0h	Host Memory Buffer Minimum Size
295:280	O	1024GB: EE77A56000h	Total NVM Capacity
		512GB: 773C256000h	
		256GB: 3B9E656000h	
		128GB: 1DCF856000h	
311:296	O	0h	Unallocated NVM Capacity
315:312	O	0h	Replay Protected Memory Block Support
317:316	O	23h	Extended Device Self-Test Time
318	O	0h	Device Self-Test Options
511:316		-	Reserved
512	M	66h	Submission Queue Entry Size Bits 7:4 – 6h Max SQES (64 bytes) Bits 3:0 – 6h Required SQES (64 bytes)
513	M	44h	Completion Queue Entry Size Bits 7:4 – 4h Max CQES (16 bytes) Bits 3:0 – 4h Required CQES (16 bytes)
515:514		0	Reserved
519:516	M	1h	Number of Namespaces
521:520	M	1Fh	Optional NVM Command Support Bits 15:6 – Reserved Bit 5 – 1h Reservations Supported 0h Not support Reservations Bit 4 – 1h Save field in Set Feature & Select field in Get Feature Supported 0h Not support Save field in Set Feature & Select field in Get Feature Bit 3 – 1h Write Zeros Supported 0h Not support Write Zeros Bit 2 – 1h Dataset Management Supported 0h Not support Dataset Management Bit 1 – 1h Write Uncorrectable Supported 0h Not support Write Uncorrectable Bit 0 – 1h Compare Supported 0h Not support Compare
523:522	M	0h	Fused Operation Support Bits 15:1 – Reserved Bit 0 – 0h Compare/Write Fused Operation Not Supported
524	M	0h	Format NVM Attributes Bits 7:3 – Reserved Bit 2 – 1h Cryptographic Erase is supprted 0h Cryptographic Erase is not supprted Bit 1 – 0h Cryptographic erase and user data erase Per Namespace Bit 0 – 0h Format Per Namespace

525	M	1h	Volatile Write Cache Bits 7:1 - Reserved Bit 0 -1h Volatile write cache is present 0h No Volatile Write Cache present
527:526	M	FFh	Atomic Write Unit Normal (0's based value)
529:528	M	0h	Atomic Write Unit Power Fail (0's based value)
530	M	1h	NVM Vendor Specific Command Configuration Bits 7:1 – reserved Bit 0 – Indicates NVM Vendor Specific Commands use the format defined in NVM Express
531	M	0h	Reserved
533:532	O	0h	ACWU
534:533	M	0h	Reserved
539:536	O	0h	No SGL support
703:540	-	0h	Reserved
I/O Command Set Attributes			
2047:704	-	0h	Reserved
Power State Descriptors			
2079:2048	M	refer to '[Table 118] Identify Power State Descriptor Structure	Power State 0 Descriptor
2111:2080	O	refer to '[Table 116] Identify Power State Descriptor Structure	Power State 1 Descriptor
2143:2112	O	refer to '[Table 116] Identify Power State Descriptor Structure'	Power State 2 Descriptor
2175:2144	O	refer to 'Identify Power State Descriptor Data Structure'	Power State 3 Descriptor
2207:2176	O	refer to 'Identify Power State Descriptor Data Structure'	Power State 4 Descriptor
...	-	0h	(N/A)
3071:3040	O	0h	Power State 31 Descriptor
Vendor Specific			
3278:3072	-	Samsung Specific	Samsung Reserved
3279	O	5h (-00000) 7h (-00007)	Security Feature Set Bit 2 – 1h TCG Supported Bit 1 – 1h SED Supported Bit 0 – 1h ATA Security Supported
4095:3280	-	0h	Samsung Reserved

[Table 118] Identify Power State Descriptor Data Structure

Bits	Power State 0	Power State 1	Power State 2	Power State3	Power State 4	Description
255:125	0h	0h	0h	0h	0h	Reserved
124:120	0h	1h	2h	3h	4h	Relative Write Latency
119:117	0h	0h	0h	0h	0h	Reserved
116:112	0h	1h	2h	3h	4h	Relative Write Throughput
111:109	0h	0h	0h	0h	0h	Reserved
108:104	0h	1h	2h	3h	4h	Relative Read Latency
103:101	0h	0h	0h	0h	0h	Reserved
100:96	0h	1h	2h	3h	4h	Relative Read Throughput
95:64	0h	0h	0h	5DCh	1770h	Exit Latency
63:32	0h	0h	0h	D2h	898h	Entry Latency
31:26	0h	0h	0h	0h	0h	Reserved
25	0h	0h	0h	1h	1h	Non-Operational State
24	0h	0h	0h	1h	1h	Max Power Scale
23:16	0h	0h	0h	0h	0h	Reserved
15:00	2F8h	258h	1FEh	190h	32h	Maximum Power

[Table 119] Identify Namespace Data Structure

Bytes	O/M	Default Value		Description
7:0	M	1024GB	733BD2B0h	Namespace Size
		512GB	3B9E12B0h	
		256GB	1DCF32B0h	
		128GB	EE7C2B0h	
15:8	M	1024GB	733BD2B0h	Namespace Capacity
		512GB	3B9E12B0h	
		256GB	1DCF32B0h	
		128GB	EE7C2B0h	
23:16	M	1024GB	733BD2B0h	Namespace Utilization
		512GB	3B9E12B0h	
		256GB	1DCF32B0h	
		128GB	EE7C2B0h	
24	M	0h		Namespace Features Bits 7:1 Reserved Bit 0: 0h Thin provisioning not supported
25	M	0h		Number of LBA Formats
26	M	0h		Formatted LBA Size Bits 7:5 – Reserved Bit 4: Metadata interleaved or separate (based on LBA format) Bit 3:0 – Indicates LBA format
27	M	0h		Metadata Capabilities Bits 7:2 – Reserved Bit 1 – Supports Metadata as separate buffer Bit 0 – Supports Metadata as extended LBA
28	M	0h		End-to-end Data Protection Capabilities Bits 7:5 – Reserved Bit 4 – Supports protection information as last 8 bytes of Metadata Bit 3 – Supports protection information as first 8 bytes of metadata Bit 2 – Supports Type 3 protection information Bit 1 – Supports Type 2 protection information Bit 0 – Supports Type 1 protection information
29	M	0h		End-to-End Data Protection Type Settings Bits 7:4 – Reserved Bit 3 – 1: Protection information transferred as first 8 bytes of metadata Bit 3 – 0: Protection information transferred as last 8 bytes of metadata Bit 2:0 – 000b: Protection information disabled Bit 2:0 – 1h: Protection type 1 enabled Bit 2:0 – 2h: Protection type 2 enabled Bit 2:0 – 3h: Protection type 3 enabled
30	O	0h		Namespace Multi-path I/O and Namespace sharing Capabilities (NMIC) Bits 7:1 - Reserved Bit 0 - 1 : Accessible by two or more controllers Bit 0 - 0 : Private namespace

31	O	0h		Reservation Capabilities (RESCAP) Bits 7 - Reserved Bits 6 - 1: Namespace supports the Exclusive Access (All Registrants reservation type) Bit 5 - 1 : Namespace supports the Write Exclusive (All Registrants reservation type) Bit 4 - 1 : Namespace supports the Exclusive Access (Registrants only reservation type) Bit 3 - 1 : Namespace supports the Write Exclusive (Registrants only reservation type) Bit 2 - 1 : Namespace supports the Exclusive Access Reservation type Bit 1 - 1 : Namespace supports the Write Exclusive Reservation type Bit 0 - 1 : Namespace supports the Persist Through Power Loss capability
32	O	80h		Bit 7 - 1:Format Progress Indicator
33		-		Reserved
35:34	O	0h		Namespace Atomic Write Unit Normal
37:36	O	0h		Namespace Atomic Write Unit Power Fail
39:38	O	0h		Namespzce Atomic Compare & Write Unit
41:40	O	0h		Namespace Atomic Boundary Size Normal
43:42	O	0h		Namespace Atomic Boundary Offset
45:44	O	0h		Namespace Atomic Boundary Size Power Fail
47:46		-		Reserved
63:48	O	1024GB	EE77A56000h	NVM Capacity
		512GB	773C256000h	
		256GB	3B9E656000h	
		128GB	1DCF856000h	
103:64		-		Reserved
119:104	O	################002538##########h (TBD)		Namespace Globally Unique Identifier (NGUID) #:Variables *NGUID specifies data in a big endian format.
127:120	O	0h (TBD)		IEEE Extended Unique Identifier(EUI64) #:Variables *EUI64 specifies data in a big endian format.
131:128	M	refer to 'LBA Format 0 Data Structure'		LBA Format 0 Support
135:132	O	0h		LBA Format 1 Support
139:136	O	0h		LBA Format 2 Support
143:140	O	0h		LBA Format 3 Support
147:144	O	0h		LBA Format 4 Support (N/A)
…				
191:188	O	0h		LBA Format 15 Support (N/A)
383:192	-	0h		Reserved
Vendor Specific				
4095:384	-	0h		Samsung Reserved

[Table 120] LBA Format 0 Data Structure

Bits	Name	Default Value	Description
31:26	-	0	Reserved
25:24	RP	0	Relative Performance
23:16	LBADS	9h	LBA Data Size
15:00	MS	0	Meta data Size

[Table 121] LBA Format 1 Data Structure

Bits	Name	Default Value	Description
31:26		0	Reserved
25:24	RP	0	Relative Performance
23:16	LBADS	Ch	LBA Data Size
15:00	MS	0	Meta data Size

6.2 NVM Express I/O Command Set

[Table 122] Opcode for NVM Express I/O Commands

Opcode (Hex)	Command Name
00h	Flush
01h	Write
02h	Read
04h	Write Uncorrectable (Not support)
05h	Compare
08h	Write Zeroes
09h	Dataset Management

NOTE:
1) Deallocate feature in Dataset Management command is only supported in the Samsung SSD PM961.

6.3 SMART/Health Information

[Table 123] SMART/Health Information Log

Bytes	Default Value	Attribute Description
0	0	Critical Warning Bit 7:5 – Reserved Bit 4 – 1h: the volatile memory backup device has failed. (only valid if the controller has a volatile memory backup solution) Bit 3 – 1h: the media has been placed in read only mode Bit 2 – 1h: the NVM subsystem reliability has been degraded due to significant media related errors or any internal error that degrades NVM subsystem reliability Bit 1 – 1h: a temperature is above an over temperature threshold or below an under temperature threshold Bit 0 – 1h: the available spare space has fallen below the threshold
2:1	current temp	Temperature
3	100	Available Spare
4	50	Available Spare Threshold
5	0	Percentage Used
31:6	-	Reserved
47:32	0	Data Units Read
63:48	0	Data Units Written
79:64	0	Host Read Commands
95:80	0	Host Write Commands
111:96	0	Controller Busy Time
127:112	0	Power Cycles
143:128	0	Power On Hours
159:144	0	Unsafe Shutdowns
175:160	0	Media and Data Integrity Errors
191:176	0	Number of Error Information Log Entries
195:192	0	Warning Composite Temperature Time
199:196	0	Critical Composite Temperature Time
201:200	current temp.	Temperature Sensor 1
203:202	0	Temperature Sensor 2
205:204	0	Temperature Sensor 3
207:206	0	Temperature Sensor 4
209:208	0	Temperature Sensor 5
211:210	0	Temperature Sensor 6
213:212	0	Temperature Sensor 7
215:213	0	Temperature Sensor 8
511:216	-	Reserved

7.0 PRODUCT COMPLIANCE

7.1 Product regulatory compliance and Certifications

[Table 124] Certifications and Declarations

Category	Certifications
Safety	c-UL-us
	CE
	TUV
	CB
EMC	CE (EU)
	BSMI (Taiwan)
	KCC (South Korea)
	VCCI (Japan)
	RCM (Australia)
	FCC (USA)
	IC (CANADA)

The three existing compliance marks (C-Tick, A-Tick and RCM) are consolidated into a single compliance mark - the RCM.

Caution: Any changes or modifications in construction of this device which are not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications, However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:
- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Modifications not expressly approved by the manufacturer could void the user's authority to operated the equipment under FCC rules.

1. 기자재 명칭 : SSD (Solid State Drive)
2. 모델명(Model): 라벨 별도 표기
3. 제조연월 : 라벨 별도 표기
4. 제조자 : 삼성전자(주)
5. 제조국가 : 대한민국
6. 상호명 : 삼성전자(주)

Industry Canada ICES-003 Compliance Label:
CAN ICES-3 (B)/NMB-3(B)

8.0 References

[Table 125] Standards References

Item	Website
PCI Express Base Specification Revision 3.0	http://www.pcisig.com/specifications/pciexpress/base3/
PCI Express CEM Specification Revision 3.0	http://pcisig.com/specifications
NVM Express Specification Rev.1.1b	http://www.nvmexpress.org/
PCIe M.2 Electromechanical Specification Revision 1.0	http://www.pcisig.com/
Solid-State Drive Requirements and Endurance Test Method (JESD218A)	http://www.jedec.org/standards-documents/docs/jesd218a
Solid-State Drive Requirements and Endurance Test Method (JESD219A)	http://www.jedec.org/standards-documents/docs/jesd219a